CLAIMS

What is claimed is:

1. An on-chip differential multiple layer inductor comprises:

first partial winding on multiple first layers, wherein the first partial winding is operably coupled to receive a first leg of a differential input;

second partial winding on the multiple first layers, wherein the second partial winding is operably coupled to receive a second leg of the differential input;

third partial winding on multiple second layers, wherein the third partial winding is operably coupled to a center tap;

fourth partial winding on the multiple second layers, wherein the fourth partial winding is operably coupled to the center tap; and

interconnecting structure operably coupled to the first, second, third, and fourth partial windings such that the first and third partial windings form a winding that is symmetrical to a winding formed by the second and fourth partial windings.

2. The on-chip differential multiple layer inductor of claim 1 further comprises:

the third partial winding being positioned with respect to the first partial winding and the fourth partial winding being positioned with respect to the second partial winding to establish a tuned capacitance such that a quality factor of the on-chip differential multiple layer inductor is optimized.

3. The on-chip differential multiple layer inductor of claim 1, wherein the interconnecting structure further comprises:

a first set of interconnections for coupling the first partial winding to the third partial winding; and

a second set of interconnections for coupling the second partial winding to the fourth partial winding, wherein the first set of interconnections is symmetrical to the second set of interconnections.

4. The on-chip differential multiple layer inductor of claim 1 further comprises at least one of:

the first partial winding including a notched corner to provide clearance for a bridge of the interconnecting structure; and

the second partial winding including a second notched corner to provide clearance for a second bridge of the interconnecting structure.

5. The on-chip differential multiple layer inductor of claim 1 further comprises:

the third partial winding having similar metalization as the first partial winding; and

the fourth partial winding having similar metalization as the second partial winding, such that yield of integrated circuits incorporating the on-chip differential multiple layer inductor increases.